The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHIN CHUNG CHEN and
FULVIO SPAGNA

Appeal No. 2003-1316
Application No. 09/430,531

ON BRIEF

Before HAIRSTON, RUGGIERO, and BLANKENSHIP, <u>Administrative Patent</u> <u>Judges</u>.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 20.

The disclosed invention relates to a delay locked loop circuit that uses a control circuit to select one of a plurality of multiplexers to pass an input signal to its output, and to prevent the input signal from passing to the outputs of the remaining plurality of multiplexers.

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Claim 1 is illustrative of the claimed invention, and it reads as follows:

- 1. An integrated delay locked loop circuit for write precompensation and clock recovery connected to receive source of multiple clock signals, each of different relative phase, comprising:
- a plurality of clock selection multiplexers each connected to receive said multiple clock signals; and

a control circuit connected to control each of said plurality of clock selection multiplexers to pass a respective selected one of said multiple clock signals to a clock selection output, wherein if one clock selection multiplexer of said plurality of clock selection multiplexers is selected to pass a particular one of said clock signals to its clock selection output, all of the remaining clock selection multiplexers of said plurality of clock selection multiplexers are prevented from passing said particular one of said clock signals to their respective clock selection outputs.

The reference relied on by the examiner is:

Hillis 5,485,627 Jan. 16, 1996

Claims 1 through 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hillis.

Reference is made to the brief (paper number 18) and the answer (paper number 19) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will sustain the anticipation rejection of claims 1 through 20.

Appellant argues (brief, page 5) that:

Hillis does not disclose or suggest the presently claimed invention including if one clock selection multiplexer of the plurality of clock selection multiplexers is selected to pass a particular one of the clock signals through the clock selection output all of the remaining clock selection multiplexers of the plurality of clock selection multiplexers are prevented from passing the particular one of the clock signals to their respective clock selection outputs as defined in independent Claims 1, 8, 14 and 18.

The Examiner alleges that control circuit 400 and multiplexer 430a and 430d discloses this aspect. There is nothing in Hillis to disclose the conditional nature of the above language.

The appellants' arguments to the contrary notwithstanding, we agree with the examiner's assessment of the teachings of Hillis (answer, pages 3 through 6). Hillis explicitly states (column 4, lines 38 through 57) that the control means or status register 400 controls the multiplexers so as to connect the host computers and the processors arrays as desired by the user by applying a selection signal to the desired multiplexer "along with a no-operation signal if no such connection is to be made." Hillis specifically states that "one" of the host computer 310A through 310D can be connected to "one" of the processor arrays 330A through 330D by selecting one multiplexer to pass signals from the host to the array (column 5, lines 34 through 42; column 7, lines 19 through 23). Thus, if one multiplexer in the plurality of

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multiplexers is selected, then a no-operation signal is sent to the other multiplexers in the plurality of multiplexers to prevent them from passing signals to their outputs.

In summary, the anticipation rejection of independent claims 1, 8, 14 and 18 is sustained because Hillis discloses "the conditional nature" of the claimed invention. The anticipation rejection of dependent claims 2 through 7, 9 through 13, 15 through 17, 19 and 20 is sustained because of the lack of patentability arguments for these claims.

DECISION

The decision of the examiner rejecting claims 1 through 20 under 35 U.S.C. § 102(b) is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR \S 1.136(a).

<u>AFFIRMED</u>

KENNETH W. HAIRSTON)
Administrative Patent Judge	∋)
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) BOARD OF PATENT
JOSEPH F. RUGGIERO) APPEALS
Administrative Patent Judge	e) AND
5) INTERFERENCES
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HOWARD B. BLANKENSHIP)
Administrative Patent Judge	· e)

KWH/lp

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